APPENDIX B

CLEAN VERSION OF SPECIFICATION

CIRCUIT OUTPUT STAGE PROTECTION SYSTEM

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention is related to NMOS-based integrated circuit (IC) output stages.

Related Art

[0002] As CMOS technology advances to the 0.1–0.2 μm range and beyond, supply voltages are scaled down accordingly. When voltage differences among the gate, source, and drain of a NMOS device exceed device ratings, the life of the device is significantly decreased. Therefore, a problem occurs when using NMOS devices in an IC output stage to interface relatively low supply voltage NMOS devices of an IC core circuit with relatively high supply voltage at the output stage.

[0003] In an example, the IC core circuit includes 0.13 μm NMOS devices that require a 1.2 V supply voltage, and the IC output stage requires a 3.3 V supply voltage. A level shifter coupled between the IC core circuit and output stage can be used to bridge the 1.2 V and 3.3 V power domains. But this approach is not advantageous because level shifters consume a significant amount of power, and combining 1.2 V IC core devices with 3.3 V output stage devices significantly increases processing cost.

[0004] What is needed, therefore, is a NMOS-based IC output stage to interface relatively low voltage NMOS devices in an IC core with relatively high voltages at the output stage, and more particularly, a system for protecting the NMOS devices in the IC output stage.

SUMMARY OF THE INVENTION

[0005] The present invention is directed to protecting NMOS devices in an IC output stage, which interfaces relatively low voltage NMOS devices in an IC core with relatively high voltages at the output stage. In an embodiment, the output stage protection system protects NMOS devices in the IC output stage during normal IC operations, IC power up/power down, and electrostatic discharge (ESD) events.

[0006] In an embodiment, the IC output stage includes a pair of relatively low voltage (e.g. 1.2 V thin oxide) NMOS devices, each having a gate coupled to an output of the IC core and a source coupled to a current source. The IC output stage further includes a first pair of relatively high voltage (e.g. 2.5 V thick oxide) NMOS devices, each having a source coupled to respective drains of the pair of 1.2 V NMOS devices. A biasing circuit biases the gates of the first pair of 2.5 V NMOS devices so that the voltage on the pair of 1.2 V NMOS devices does not exceed the voltage rating for 1.2 V NMOS devices. A second pair of relatively high voltage (e.g. 2.5 V thick oxide) NMOS devices each have a source coupled to respective drains of the first pair of 2.5 V NMOS devices and a drain coupled to a first output node and a second output node, respectively.

[0007] The IC output stage further includes one or more diodes coupled in series between the first output node and the gates of the second pair of 2.5 V NMOS devices, and one or more diodes coupled in series between the second output node and the gates of the second pair of 2.5 V NMOS devices. The series diodes substantially ensure that the first and second pairs of 2.5 V NMOS devices and the pair of 1.2 V NMOS devices operate within the device ratings during IC power up/power down. In another embodiment, the series diodes are coupled to the gates of the second pair of 2.5 V NMOS devices through a resistor. The series diodes, in conjunction with the resistor, provide added protection during ESD events at the output nodes.

[0008] In an embodiment, an output stage protection system protects NMOS devices in an IC output stage from ESD events at the input/output (I/O) pads. A first I/O pad ESD protection circuit is coupled to a first I/O pad and a second I/O pad ESD protection circuit is coupled to a second I/O pad. The first and second I/O pad ESD protection circuits include a clamp coupled to a local net as opposed to a chip-level supply voltage. The clamp redirects ESD to ground, away from the NMOS devices of the output stage.

[0009] In another embodiment, the IC output stage has a single-ended configuration. A relatively low voltage NMOS device is coupled to an IC core output and to a current source. A first relatively high voltage NMOS device is coupled to a biasing circuit and to the relatively low voltage NMOS device. A second relatively high voltage NMOS device is coupled to an output node and to the first relatively high voltage NMOS device. The single-ended IC output stage further includes one or more diodes coupled between the output node and a gate of the second relatively high voltage NMOS device. The one or more diodes substantially ensure that the first and second relatively high voltage NMOS devices and the relatively low voltage NMOS device operate within the device ratings during IC power up/power down. The one or more diodes are optionally coupled to the gate of the second relatively high voltage NMOS device through a resistor for added protection during ESD events at the output node.

[0010] Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to accompanying drawings. It is noted that the invention is not limited to the specific embodiments described herein. Such embodiments are presented for illustrative purposes only. Additional embodiments will be apparent to persons skilled in the relevant arts based on the teachings contained herein.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0011] The present invention will be described with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost digit(s) in the corresponding reference number.

[0012] FIG.1 illustrates a block diagram of a system for interfacing relatively low voltage devices in an IC core with relatively high voltage at an output stage.

[0013] FIG. 2 illustrates a circuit diagram of an output stage protection system, which protects NMOS devices in an IC output stage during normal IC operations.

[0014] FIG. 3 illustrates a circuit diagram of an output stage protection system, in accordance with an embodiment of the present invention, which protects NMOS devices in an IC output stage during normal IC operations and IC power up/power down.

[0015] FIG. 4 illustrates an example NMOS diode implementation for the output stage protection system shown in FIG. 3.

[0016] FIG. 5 illustrates an IC input/output (I/O) pad circuit, which provides local electrostatic discharge (ESD) protection, in accordance with an embodiment of the present invention.

[0017] FIG. 6 illustrates a circuit diagram of an output stage protection system, in accordance with an embodiment of the present invention, which protects NMOS devices in an IC output stage during normal IC operations and IC power up/power down, and provides local ESD protection at the I/O pads.

DETAILED DESCRIPTION OF THE INVENTION

Overview

[0018] The present invention is directed to protecting NMOS devices in an IC output stage, which interfaces relatively low voltage NMOS devices in an IC

core with relatively high output voltages at the output stage. In the detailed description that follows, the preferred embodiments of the present invention are presented in detail. While specific features, configurations, and devices are discussed in detail, this description is for illustrative purposes, and persons skilled in the art will recognize that other configurations and devices can be used to achieve the features of the present invention without departing from the scope and spirit thereof.

Example Output Stage System

[0019] FIG.1 illustrates a block diagram of an example system 100 for interfacing relatively low voltage devices in an IC core with relatively high voltages at an output stage. In system 100, a level shifter 104 bridges a relatively low voltage core 102 with a relatively high voltage output 106. For exemplary purposes, the relatively low voltage core 102 is described herein as a 1.2 V core. The relatively high voltage output is described herein as a 3.3 V output. The invention is not, however, limited to these example voltages. Based on the description herein, one skilled in the relevant art(s) will understand that the invention can be implemented with other voltage levels.

[0020] Disadvantages of system 100 are level shifter 104 consumes a significant amount of power, and combining 1.2 V devices in IC core 102 with 3.3 V devices in output stage 106 significantly increases processing cost or are not available in the technology.

NMOS-based Output Stage Protection System for Normal IC Operations

[0021] FIG. 2 illustrates a circuit diagram of a NMOS-based output stage protection system 200, which interfaces relatively low supply voltage NMOS devices in an IC logic core 201 with relatively high supply voltages at an output stage 202. Advantageously, NMOS-based output stage protection system 200 does not require a level shifter, such as level shifter 104, shown in FIG. 1. During normal IC operations, output stage protection system 200 of

FIG. 2 protects 1.2 V NMOS main output stage devices and 2.5 V NMOS output stage protection devices in output stage 202.

[0022] In output stage 202, a pair of 1.2 V NMOS devices M1 204 and M2 206 each have a gate coupled to respective outputs of IC logic core 201, and a source coupled to a current source 208. A first pair of 2.5 V NMOS cascode devices M3 210 and M4 212 each have a source coupled to respective drains of 1.2 V pair M1 204 and M2 206. First pair M3 210 and M4 212 each have a gate coupled to an external biasing circuit 214, which biases first pair M3 210 and M4 212 so that 1.2 V pair M1 204 and M2 206 operate in the saturation region. External biasing circuit 214 biases the gates of first pair M3 210 and M4 212 such that a gate-source voltage difference at the drains of 1.2 V pair M1 204 and M2 206 does not exceed approximately 1.2 V. Methods and systems for implementing external biasing circuit 214 are well known to one skilled in the relevant art(s).

[0023] A second pair of 2.5 V NMOS cascode devices M5 216 and M6 218 each have a source coupled to respective drains of first pair M3 210 and M4 212. Gates of second pair M5 216 and M6 218 are coupled together and biased to approximately 2.5 V in order to bias first pair M3 210 and M4 212 in the saturation region. 2.5 V cascode device M5 216 has a drain coupled to an output node A 220, and 2.5 V cascode device M6 218 has a drain coupled to an output node B 222. In an embodiment, output nodes A 220 and B 222 are referenced to a 3.3 V external voltage supply through a resistive load.

[0024] In an embodiment, output stage protection system 200 has a single-ended configuration. A relatively low voltage NMOS device replaces pair of 1.2 V NMOS devices M1 204 and M2 206. A first relatively high voltage NMOS device replaces first pair of 2.5 V NMOS cascode devices M3 210 and M4 212, and a second relatively high voltage NMOS device replaces second pair of 2.5 V NMOS cascode devices M5 216 and M6 218.

[0025] Output stage protection system 200 ensures that during normal IC operations, first and second pairs of cascode devices M3 210-M6 218 and 1.2 V pair M1 204 and M2 206 operate in a relatively safe region, within the

voltage ratings of the devices. For example, the voltage difference between any two of the three terminals (gate, source, and drain) of a 1.2 V NMOS device should not exceed approximately 1.32 V and the voltage difference between any two terminals of a 2.5 V NMOS device should not exceed approximately 2.75 V.

[0026] A problem occurs, however, during IC power up/power down when the NMOS device supply voltages are slowly ramping up or down. For example in FIG. 2, when 2.5 V supply voltage 224 and 1.2 V supply voltage 226 are slowly ramping up or down, and output nodes A 220 and B 222 are referenced to a 3.3 V external supply voltage, gate voltages of first and second pairs of cascode devices M3 210-M6 218 are approximately 0 V. Therefore, during IC power up/power down, the drain-source voltage difference between first and second pairs of cascode devices M3 210-M6 218 is about 3.3 V, which exceeds the 2.75 V voltage rating of the devices.

NMOS-based Output Stage Protection during IC Power Up/Power Down

[0027] FIG. 3 illustrates a circuit diagram of a NMOS-based output stage protection system 300, in accordance with an embodiment of the present invention. Output stage protection system 300 interfaces relatively low supply voltage NMOS devices in IC logic core 201 with relatively high supply voltages in an output stage 301, and protects NMOS devices in output stage 301 during normal IC operations, as described in conjunction with FIG. 2 above.

[0028] Output stage protection system 300 differs from output stage protection system 200, shown in FIG. 2, in that the gates of second pair of cascode devices M5 216 and M6 218 in FIG. 3 are coupled to output pads A 220 and B 222 through series diodes. The series diodes are configured to protect NMOS devices in output stage 301 during IC power up/power down. In an embodiment, the gates of second pair of cascode devices M5 216 and M6 218 in FIG. 3 are coupled to output pads A 220 and B 222 through a resistor and series diodes. The resistor and series diodes are configured to

protect NMOS devices in output stage 301 during IC power up/power down, as well as during ESD events on output nodes A 220 and B 222.

[0029] In FIG. 3, output stage 301 includes a first set of diodes 302 coupled between output node A 220 and a resistor R0 306, and a second set of diodes 304 coupled between output node B 222 and resistor R0 306. Resistor R0 306 is coupled between first and second sets of diodes 302 and 304 and the gates of second pair of cascode devices M5 216 and M6 218. In the example of FIG. 3, each set of diodes 302 and 304 includes a pair of diodes, for a total of four diodes. The number of diodes coupled in series between output nodes A 220 and B 222 can, however, be greater or fewer than four.

[0030] First and second sets of diodes 302 and 304 protect NMOS devices M1 204-M6 218 during IC power up/power down, and in conjunction with resistor R0 306, also protect NMOS devices M1 204-M6 218 during ESD events on output nodes A 220 and B 222. For example, the drain-gate voltage difference of a 2.5 V NMOS device should not exceed the device voltage rating of approximately 2.75 V. During IC power up/power down and during ESD events, the voltage on output nodes A 220 and B 222 may, at times, exceed 3.3 V, and the drain-gate voltage difference of second pair of cascode devices M5 216 and M6 218 may, at times, exceed 2.75 V.

[0031] In the example of FIG. 3, when the voltage on output nodes A 220 and B 222 exceeds 3.3 V, first and second pairs of diodes 302 and 304 are forward-biased. First and second pairs of diodes 302 and 304 pull up the gate voltage of second pair of cascode devices M5 216 and M6 218 so that the drain-gate voltage difference of the devices is below the device voltage rating of approximately 2.75 V. The source voltage of second pair of cascode devices M5 216 and M6 218 will also be pulled up so that the gate-source voltage difference of the devices is approximately equal to 2.75 V. During an ESD event on output nodes A 220 and B 222, resistor R0 306, in conjunction with first and second diode pairs 302 and 304, functions as a low-pass filter and further protects the gates of second pair of cascode devices M5 216 and M6 218.

[0032] In another embodiment, output stage 301 has a single-ended configuration. A relatively low voltage NMOS device replaces pair of 1.2 V NMOS devices M1 204 and M2 206. A first relatively high voltage NMOS device replaces first pair of 2.5 V NMOS cascode devices M3 210 and M4 212, and a second relatively high voltage NMOS device replaces second pair of 2.5 V NMOS cascode devices M5 216 and M6 218. A set of one or more diodes replaces first and second diode pairs 302 and 304. The set of one or more diodes is coupled between an output node and a gate of the second relatively high voltage NMOS device to protect the NMOS devices in output stage 301 during IC power up/power down. The set of one or more diodes is optionally coupled to the gate of the second relatively high voltage NMOS device through a resistor for added ESD protection.

[0033] FIG. 4 illustrates an example NMOS diode implementation for the diodes of first and second diode pairs 302 and 304, shown in FIG. 3. In the example of FIG. 4, a diode PN junction is implemented from a P+ area 402 and an N-Well area 404 of a PNP structure 400. A guard ring 408 surrounding PNP structure 400 is coupled to contacts on a P-substrate 406 in order to prevent latch up. Alternative diode structures can also be used to implement the diodes of first and second diode pairs 302 and 304.

I/O Pad Local ESD Protection System

[0034] FIG. 5 illustrates an input/output (I/O) pad ESD protection system 500, in accordance with an embodiment of the present invention, which provides local ESD protection at an I/O pad 502. I/O diode pairs D0 506 and D1 508 and D2 510 and D3 512 are coupled to a local net Avddlocal 504 and a separate ESD clamp 501, as opposed to a chip-level ESD protection circuit and power bus.

[0035] In FIG. 5, local net Avddlocal 504 is coupled to I/O pad 502 in parallel with clamp 501. Clamp 501 includes a resistor 516 coupled between local net Avddlocal 504 and an input of an inverter 518. A capacitor 522 is coupled between the input of inverter 518 and a ground 514. A NMOS device 520 has

a gate coupled to an output of inverter 518, a drain coupled to local net Avddlocal 504, and a source coupled to ground 514. When an ESD event occurs on I/O pad 502, diode pair D0 506 and D1 508 are forward biased, and clamp 501 discharges ESD voltage to ground 514. A resistor Rd 524 ensures that local net Avddlocal 504 is less than approximately 2.75 V during normal operation in order to protect NMOS device 520 in clamp 501.

[0036] I/O pad ESD protection system 500 can be implemented in conjunction with NMOS-based output stage protection system 300, shown in FIG. 3. For example, FIG. 6 illustrates a circuit diagram of an output stage protection system 600, in accordance with an embodiment of the present invention. Output stage protection system 600 protects NMOS devices in output stage 301 during normal IC operations, IC power up/power down, and ESD events on output nodes A 220 and B 222, as described in conjunction with FIGS. 2-3 above.

[0037] Output stage protection system 600 also provides local ESD protection at first and second I/O pads 502 and 602. Output stage 301 interfaces 1.2 V IC logic core 201 with an external 3.3 V supply voltage 601. A first I/O pad local ESD protection circuit 604 is coupled to first I/O pad 502, and a second I/O pad local ESD protection circuit 606 is coupled to second I/O pad 602. First and second I/O pad local ESD protection circuits 604 and 606 have the configuration of I/O pad ESD protection system 500, shown in FIG. 5. First and second I/O pad local ESD protection circuits 604 and 606 protect first and second I/O pads 502 and 602 from ESD events without exceeding the device voltage ratings of NMOS devices M1 204-M6 218 in output stage 301.

Conclusion

[0038] The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and

relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by discrete components, application specific ICs, processors executing appropriate software and the like or any combination thereof.

[0039] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.